IN THE CLAIMS:

Please cancel claim 2 in its entirety without prejudice nor disclaimer of the subject matter set forth therein.

Please amend claims 1, 3-6 and 11 and add new claims 12-23 as follows.

1. (Currently Amended) A semiconductor memory device comprising:

a plurality of memory blocks;

a plurality of signal lines respectively connected to said ~~plurality of~~ memory blocks; and

a control circuit connected to said signal lines, said control circuit including a plurality of selection signal generator circuits ~~for~~ generating a plurality of generating selection signals for selecting one ~~memory block~~ of said ~~plurality of~~ memory blocks by an externally input address ~~signals~~ signal and for outputting said selection signals to said signal lines,

wherein lengths of the signal lines from said selection signal generator circuits to the respective memory blocks are longer in proportion to distances from said control circuit to said memory blocks, and

wherein driving capabilities of said selection signal generator circuits are larger in proportion to the distances from said control circuit to said memory blocks.

2. (Cancelled)

3. (Currently Amended) A semiconductor memory device according to Claim 1 ~~2~~, wherein differences between driving capabilities of said selection signal generator circuits ~~for outputting said selection signals to said signal lines~~ are determined by ratios of lengths of said signal lines connected to said control circuit.

4. (Currently Amended) A semiconductor memory device ~~according to Claim 1,~~ comprising:

a plurality of memory blocks;

a plurality of signal lines respectively connected to said memory blocks; and

a control circuit connected to said signal lines, said control circuit including a plurality of selection signal generator circuits generating a plurality of generating selection signals for selecting one of said memory blocks by an externally input address signal and for outputting said selection signals to said signal lines,

wherein lengths of the signal lines from said selection signal generator circuits to the respective memory blocks are longer in proportion to distances from said control circuit to said memory blocks, and

wherein gate widths of transistors that constitute said selection signal generator circuits are longer in proportion to the distances from said control circuit to said memory blocks.

5. (Currently Amended) A semiconductor memory device according to Claim 4, wherein differences between the gate widths of transistors that constitute said selection signal generator circuits ~~for outputting said selection signals to the respective signal lines~~ are determined by ratios of lengths of said signal lines connected to said control circuit.

6. (Currently Amended) A semiconductor memory device ~~according to Claim 1,~~ comprising:

a plurality of memory blocks;

a plurality of signal lines respectively connected to said memory blocks; and

a control circuit connected to said signal lines, said control circuit including a plurality of selection signal generator circuits generating a plurality of generating selection signals for selecting one of said memory blocks by an externally input address signal and for outputting said selection signals to said signal lines,

wherein lengths of the signal lines from said selection signal generator circuits to the respective memory blocks are longer in proportion to distances from said control circuit to said memory blocks, and

wherein said selection signal generator circuits are constituted by NAND circuits with said address signals as input.

7. (Original) A semiconductor memory device according to Claim 1, wherein said control circuit further includes a signal driver circuit for transmitting said selection signals to the respective memory blocks.

8. (Original) A semiconductor memory device according to Claim 7, wherein driving capability of said signal driver circuit is larger in proportion to the distances from said control circuit to said memory blocks.

9. (Original) A semiconductor memory device according to Claim 7, wherein gate widths of transistors that constitute said signal driver circuit are longer in proportion to the distances from said control circuit to said memory blocks.

10. (Original) A semiconductor memory device according to Claim 7, wherein said signal driver circuit is constituted by inverters with output of said selection signal generator circuits as input.

11. (Currently Amended) A semiconductor memory device comprising:

a plurality of memory blocks disposed along a first direction;

a plurality of signal lines respectively connected to said ~~plurality of~~ memory blocks; and

a control circuit disposed apart from said ~~plurality of~~ memory blocks along said first direction and connected to said signal lines, said control circuit including a plurality of selection signal generator circuits ~~for~~ generating a plurality of selection signals for selecting one ~~memory block~~ of said ~~plurality of~~ memory blocks by an externally input address signal ~~signals~~ and for outputting said selection signals to said signal lines,

wherein lengths of said signal lines from said selection signal generator circuits to the respective memory blocks are longer in proportion to distances from said control circuit to said memory blocks, and

wherein driving capabilities of said selection signal generator circuits are larger in proportion to the distances from said control circuit to said memory blocks.

12. (New) A semiconductor memory device according to Claim 11, wherein said control circuit further includes a signal driver circuit for transmitting said selection signals to the respective memory blocks.

13. (New) A semiconductor memory device according to Claim 12, wherein driving capability of said signal driver circuit is larger in proportion to the distances from said control circuit to said memory blocks.

14. (New) A semiconductor memory device according to Claim 12, wherein gate widths of transistors that constitute said signal driver circuit are longer in proportion to the distances from said control circuit to said memory blocks.

15. (New) A semiconductor memory device according to Claim 12, wherein said signal driver circuit is constituted by inverters with output of said selection signal generator circuits as input.

16. (New) A semiconductor memory device according to Claim 4, wherein said control circuit further includes a signal driver circuit for transmitting said selection signals to the respective memory blocks.

17. (New) A semiconductor memory device according to Claim 16, wherein driving capability of said signal driver circuit is larger in proportion to the distances from said control circuit to said memory blocks.

18. (New) A semiconductor memory device according to Claim 16, wherein gate widths of transistors that constitute said signal driver circuit are longer in proportion to the distances from said control circuit to said memory blocks.

19. (New) A semiconductor memory device according to Claim 16, wherein said signal driver circuit is constituted by inverters with output of said selection signal generator circuits as input.

20. (New) A semiconductor memory device according to Claim 6, wherein said control circuit further includes a signal driver circuit for transmitting said selection signals to the respective memory blocks.

21. (New) A semiconductor memory device according to Claim 20, wherein driving capability of said signal driver circuit is larger in proportion to the distances from said control circuit to said memory blocks.

22. (New) A semiconductor memory device according to Claim 20, wherein gate widths of transistors that constitute said signal driver circuit are longer in proportion to the distances from said control circuit to said memory blocks.

23. (New) A semiconductor memory device according to Claim 20, wherein said signal driver circuit is constituted by inverters with output of said selection signal generator circuits as input.